A NOVEL ALGORITHM FOR BIAS-DEPENDENT CASCODE FET MODELING

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ABSTRACT

In this work, we present a novel algorithm for a flexible table-based, bias-dependent, small-signal cascode MESFET model. The model utilizes 2-port D.C. and R.F. characterizations of a single-gate, common-source MESFET in contrast to the typical 3-port characterization approach typically applied to dual-gate and cascode FETs. Cascode FET simulations enabled by the new model are shown to track measured data over varying bias conditions.

INTRODUCTION

Cascode connected MESFETs (hereafter referred to as cascode FETs) like their dual-gate FET cousins have found a variety of uses in microwave applications; two examples of which are gain controlled amplifiers and phase shifters. The physical difference between a dual-gate FET and a cascode FET is that the dual-gate FET is fabricated as one device with two gates whereas the cascode FET is a cascode connection of two single-gate FETs. Although the devices are physically different, both devices are modeled as two single-gate FETs connected in cascode, see Figure 1 [1]. Since the advantage of using a dual-gate FET or a cascode FET is the capability to control device gain as a function of the second gate voltage, designers need a bias-dependent small-signal model which will allow them to predict the change in circuit performance (e.g., gain and phase shift) as a function of the second gate voltage.

Bias-dependent dual-gate FET models have been published in the literature [1], [2]. The model described by Asai, et. al., [1] is a physics-based model. Physics-based models are difficult to work with since they require detailed information about semiconductor parameters, which may not be readily available, and they often do not accurately track measured data due to idealizations inherent in the models. More recently, Schoon [2] has described an empirical bias-dependent small-signal model for the dual-gate FET. The model consists of two single-gate, nonlinear FET models connected in cascode. Determination of the dual-gate model parameters is accomplished by a complicated optimization procedure requiring D.C. I-V data and 3-port S-parameters at multiple bias points. Although not a bias-dependent model, Tsironis [3] has described a graphical technique that makes the D.C. characteristic of the dual-gate and cascode FETs easier to understand.

In this work, a novel algorithm is presented for a bias-dependent, small-signal cascode MESFET model, based on 2-port characterization techniques. In comparison, the disadvantages of the existing direct 3-port characterization techniques include increased R.F. measurement complexity, the need to characterize over a 3-D bias plane (V_{ds}, V_{gs1}, and V_{gs2}), and the non-existence of direct parameter extraction techniques for the full cascode (or dual-gate) FET model.

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The present technique avoids these difficulties. The model is based on 2-port DC and R.F. characterizations of a separately fabricated common-source MESFET. The common-source MESFET is similar in geometry to the two single gate FETs comprising the cascode FET, but much easier to model. Direct parameter extraction techniques [4, 5] are used to extract small-signal models of the common-source FET over a 2-D bias plane. The modeling algorithm described below uses this data to produce a very flexible table-based model that allows 2-port and 3-port cascode performance to be predicted as a function of all three external cascode bias voltages.

COMBINED D.C./R.F. MODELING ALGORITHM

The small-signal model used for the common-source MESFET is shown in Figure 2. The first step is to measure the D.C. I-V transfer curve of a single gate common-source FET. The D.C. I-V data are then modeled by the following equation [6]:

$$\begin{aligned} I_d(V_{gs},V_{ds}) = & \frac{I_{\max}}{2} \cdot \\ & \left\{1+\tanh\left(a\cdot V_{gs}+b\right)\right\}\cdot \\ & \left\{\tanh\left(e\cdot V_{ds}\cdot\exp\left(c\cdot V_{gs}\right)\right)\right\}+ \\ & f\cdot V_{ds}\cdot\left\{1+\tanh\left(g\cdot V_{gs}+i\right)\right\} \end{aligned} \quad (1)$$

where I_{max} and a through h denote fitting coefficients.

Next, Cold-FET (V_{ds} = 0 V, V_{gs} > 0.7 V) and Pinched-FET (V_{ds} = 0 V, V_{gs} < 1.0 V) S-parameters are measured to extract values for the ECPs of the small-signal model (i.e., Ls, Ld, Lg, Rs, Rd, Rg, Cpg, and Cpd) [4, 5]. Finally, Hot-FET (V_{ds} > 0 V) S-parameters of the FET are measured over an equally spaced grid of bias points. Intrinsic ECPs are extracted at each bias point [4]. The bias-dependent intrinsic ECPs are stored and form the basis for a table-based small-signal FET model [7]. The table-based model performs 2-D linear interpolation on stored ECP values, enabling simulations at any chosen bias point for the common-source MESFET.

The complete cascode FET model is formed by directly connecting two small-signal models together in the cascode fashion as in Figure 1b. The indefinite admittance matrix formulation employed [8] allows the FET terminals of the second device to be translated from a common-source to a common-gate configuration. The D.C. operating point of each of the individual devices composing the cascode model is determined using the method described below.

SOLUTION FOR INTERNAL CASCODE FET BIAS VOLTAGES

A numerical D.C. solution to the internal cascode FET bias conditions is one of the important advances incorporated in the cascode model algorithm. The problem is to determine the internal operating bias voltages applied to each individual device in the cascode for a given set of external bias voltages. The solution proceeds as follows. Examining Figure 1a, the following conditions are true of the cascode FET:

$$I_{d1}(V_{gs1},V_{ds1}) = I_{d2}(V_{gs2},V_{ds2}) \quad (2)$$

$$V_{ds2} = V_{ds} - V_{ds1} \quad (3)$$

$$V_{gs2} = V_{g2} - V_{ds1} \quad (4)$$

and

$$V_{g1} = V_{gs1} \quad (5)$$

Substituting Eqs. (3)-(5) into Eq. (2) we have

$$I_{d1}(V_{g1},V_{ds1}) - I_{d2}(V_{g2}-V_{ds1},V_{ds}-V_{ds1}) = 0 \quad (6)$$

Note that there is only one unknown in Eq. (6), V_{ds1}. If Eq. (1) is substituted for the drain current of each device in Eq. (6), the result is a

transcendental equation with V_{ds1} being the unknown. The cascode model algorithm uses a numerical method (a combination of the bisection and secant method [9]) to solve Eq. (6) for V_{ds1}. Once V_{ds1} is known Eqs. (3)-(5) can be used to calculate the other internal bias voltages.

Once each pair of voltages (V_{gs1}, V_{ds1}) and (V_{gs2}, V_{ds2}) are known, intrinsic element values of the model are calculated using the table-based model. Analytical indefinite Y-parameter equations of the cascode FET are used to calculate either the 3-port or the 2-port response.

RESULTS

While the above described algorithm is general and could be ported to any microwave CAD tool, in this work it was implemented as a user defined model in HP-EESOF's Libra IV™ software. The accuracy of the model was checked by comparing the model's 2-port S-parameters to the measured 2-port S-parameters of the cascode FET at various bias points. Comparisons of model and data at two different bias points are shown in Figures 3a and 3b. It can be seen that the model tracks the data fairly well.

In the figures, note that the measured magnitude of S_{22} is greater than one. This indicates that the 2nd port of the device exhibits a negative resistance and the device could oscillate. This response is expected and is believed to be caused by the common-gate configuration of the second FET. Note that the model also tracks the device's S_{22} response.

It has been observed that at some bias points improvements may be possible in the model's fit to cascode data. Recall, however, that the model is constructed entirely of extracted data on individual common-source FETs, without any optimization to measured cascode FET data. Improvements to data fit may be made by adjusting a subset of the cascode model parameters.

SUMMARY

A bias-dependent small-signal model of a cascode FET based on 2-port D.C. and R.F. characterizations of a separately fabricated common-source MESFET has been presented. The cascode FET model is formed by connecting two bias-dependent FET models in cascode. Comparisons of model to measured cascode FET data show that the model fits the data fairly well, although further refinements can be made by utilizing the cascode FET data.

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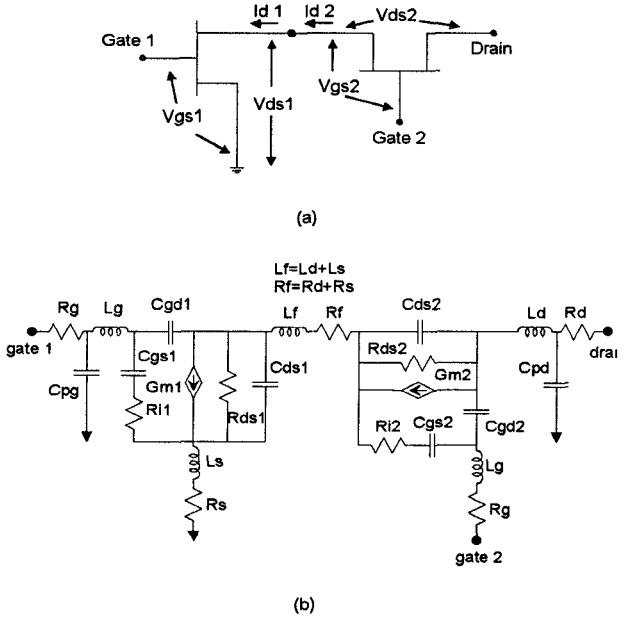

Figure. 1: (a) Schematic of cascode FET model. (b) Complete small-signal model of cascode FET.

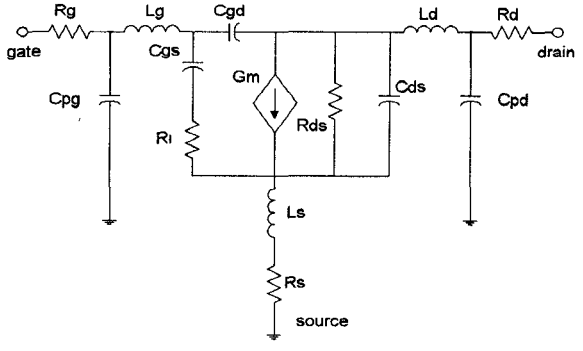

Figure 2: Small-signal model of common-source MESFET.

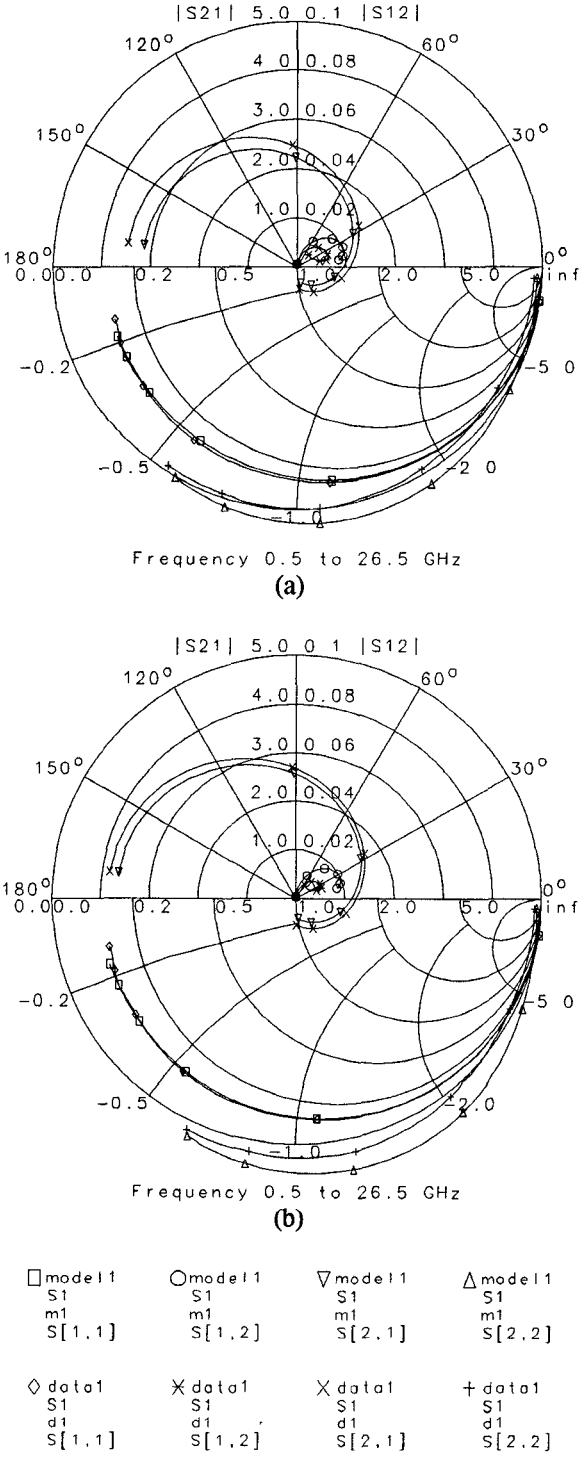

Figure 3: Comparison of cascode FET model versus measured data: (a) at V_{g1} = -0.6 V, V_{g2} = 2.980 V, V_d = 1.5 V; (b) at V_{g1} = -0.4 V, V_{g2} = 2.632 V, V_d = 3.0 V.